Planar Transformers

Field of the Invention

The present invention relates to transformer structures suitable for integrated circuits.

Background to the Invention

On-chip transformers are relatively rare in silicon RF integrated circuits and make use of a few well-known layout techniques, e.g. placing the primary and secondary windings one above the other in different interconnect layers. While some of these techniques ensure symmetry in the sense that the primary and secondary parts are identical. Generally, however, the two inductors are not balanced.

A more symmetrical layout comprises inward and outward spiralling paths which cross twice in all but the outer and inner turns which contain only one crossing. Transformers employing such symmetrical inductors are shown in Simburger, W. et al., "A Monolithic 3.7W Silicon Power Amplifier with 59% PAE at 0.9GHz", 1999 IEEE International Solid-State Circuits Conference, TP 13.6. These transformers comprise the turns of each inductor arranged in one or more blocks, which are arranged coaxially.

The Simburger transformers have a complex layout and are undesirably lossy. Furthermore, it is difficult to match the electrical properties of the windings.

Summary of the Invention

It is an object of the present invention to provide an improved substantially planar transformer suitable for use in integrated circuits.

According to the present invention, there is provided a substantially planar transformer comprising a plurality of windings and having an intermingled portion in which at least a portion of a first winding is intermingled with at least a portion of at least a second winding, wherein each full turn of each winding in said

intermingled portion is effected by one self-crossing and two crossings of each other winding having turns in said intermingled portion.

In a transformer having a first winding and a second winding, both windings having the same number of turns, the intermingled region preferably comprises substantially the whole of both windings.

In a transformer having a first winding and a second winding, the first winding having a greater number of turns than the second winding, excess turns of the first winding can encompass the intermingled region and/or be encompassed by the intermingled region.

A transformer may have an intermingled region including turns of three or more windings.

According to the present invention there is provided an integrated circuit including a substantially planar transformer according to the present invention.

Preferably, the turns of said transformer are formed from a plurality of stacked conductive paths, the paths forming each winding being united by vias. More preferably, at least one of said crossings comprises first and second bridges between radially separated conductors, the bridges being between conductive paths in respective layers and crossing each other. Still more preferably, at said at least one of said crossings, the conductors in a layer which are not connected to a bridge also in that layer are chamfered to provide a terminal edge lying parallel to a side edge of the bridge in the same layer.

Preferably, uniting vias are located adjacent to said crossings.

Preferably, a lower conductor layer forming a capacitive shield at said crossings is included. More preferably, said lower conductor layer does not contain any bridges and comprises two opposed pairs of parallel fingers terminating close together under each crossing.

Preferably, a ground shield is included underlying the transformer. More preferably, the ground shield comprises a plurality of substantially radially extending fingers, the fingers being connected by a broken ring. Still more preferably, the ring is located inwards from the outer periphery of the ground shield such that the transformer's magnetic field is substantially parallel to the integrated circuit's surface at the broken ring.

Brief Description of the Drawings

Figure 1 is a plan view of a 1:1 ratio transformer according to the present invention;
Figure 2 is a plan view showing the primary winding only of the transformer of Figure 1;
Figure 3 is a plan view showing the secondary winding only of the transformer of Figure 1;
Figure 4 is a sectional view along AA of a cross-over of the transformer of Figure 1;
Figure 5 is an exploded view of a cross-over of the transformer of Figure 1;
Figure 6(a) illustrates a layer of a crossover of the transformer of Figure 1 and
Figure 6(b) illustrates a layer of a conventional crossover;
Figure 6(c) illustrates a layer of an alternative crossover for a transformer according to the present invention;
Figure 7 is a plan view of the shield underlying the transformer of Figure 1;
Figure 8 illustrates a second transformer according to the present invention;
Figure 9 illustrates a third transformer according to the present invention;
Figure 10 illustrates a fourth transformer according to the present invention; and
Figure 11 illustrates a fifth transformer according to the present invention;

Detailed Description of the Preferred Embodiments

Preferred embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings.

Referring to Figures 1, 2, 3 and 4, an on-chip planar transformer 1 is formed in metal interconnect layers of a silicon integrated circuit 2. The transformer 1